

PATENT
W&B Ref. No. : INF 2003-US/PC
Atty. Dkt. No. INFNWB0035

IN THE CLAIMS:

The listing of claims remains as follows:

1-10 (Canceled)

11. (Previously Presented) A memory cell formed on a substrate, comprising:
a trench capacitor; and
a select transistor, comprising:
a diffusion region forming a source/drain electrode of the select transistor,
a bit-line contact formed in an insulator layer and comprising a filling
comprising at least one of a metal and a metal alloy, wherein the bit-line contact
connects the source/drain electrode to an associated bit line; and
a doped region formed within the source/drain electrode, wherein the
doped region is completely surrounded by the source/drain electrode except for a
surface to contact the filling of the bit-line contact, the doped region comprising a
locally limited electrically conductive contact layer which is formed substantially
underneath the bit-line contact in the diffusion region and which has substantially
no lateral migration underneath the insulator layer adjoining the bit-line contact.

12-13. (Canceled)

14. (Original) The memory cell of claim 11, wherein the select transistor is at
least partially disposed in the substrate and the trench capacitor is completely disposed
in the semiconductor substrate.
15. (Original) The memory cell of claim 11, wherein the bit-line contact comprises
at least one of tungsten, aluminum and copper.
16. (Previously Presented) The memory cell of claim 11, wherein the memory cell
is part of a memory cell arrangement comprising peripheral contacts formed in a same
structure plane and comprising a filling substantially similar to that of the bit-line contact.

PATENT
W&B Ref. No. : INF 2003-US/PC
Atty. Dkt. No. INFNWB0035

17. (Original) The memory cell of claim 11, the bit-line contact further comprising a liner layer formed between the substrate and the filling of the bit-line contact.
18. (Original) The memory cell of claim 17, wherein the liner layer comprises at least one of Ti and Ti/TiN.
19. (Previously Presented) A memory cell formed on a substrate, comprising:
a trench capacitor; and
a select transistor, comprising:
a diffusion region forming a source/drain electrode of the select transistor;
a bit-line contact formed in an insulator layer and comprising a filling comprising at least one of a metal and a metal alloy, wherein the bit-line contact connects the source/drain electrode to an associated bit line;
a doped region formed within the source/drain electrode between the substrate and the filling of the bit-line contact, wherein the doped region is completely surrounded by the source/drain electrode except for a surface to contact the filling of the bit-line contact, the doped region comprising a locally limited electrically conductive contact layer which is formed substantially underneath the bit-line contact in the diffusion region and which has substantially no lateral migration underneath the insulator layer adjoining the bit-line contact;
and
an annealed region formed as a result of an anneal process performed during fabrication of the bit-line contact.
20. (Original) The memory cell of claim 19, wherein the annealed region includes a damaged region damaged during a doping process performed to form the doped region.
21. (Original) The memory cell of claim 19, wherein the annealed region includes at least a portion of the doped region.
22. (Original) The memory cell of claim 19, the bit-line contact further comprising a liner layer formed between the substrate and the filling of the bit-line contact.

PATENT
W&B Ref. No. : INF 2003-US/PC
Atty. Dkt. No. INFN/WB0035

23. (Previously Presented) The memory cell of claim 22, wherein the liner layer comprises at least one of Ti and Ti/TiN.

24. (Previously Presented) The memory cell of claim 19, wherein another source/drain electrode of the select transistor is connected to an electrode of the trench capacitor which is completely disposed in the substrate.